ence ground plane can be formed either on the back side of the substrate, or on the same side of the substrate as the polygonal regions and sense regions but separated from the polygonal regions and sense regions by a dielectric, or on a separate substrate. In a self-capacitance touch screen, each touch pixel or sensor has a self-capacitance to the reference ground that can be changed due to the presence of a finger. A touch screen can use both mutual and self-capacitance measurements in a time-multiplexing fashion to gather additional information and each measurement type can compensate the weaknesses of the other.

[0118] Example displays including pixels with dual-function capacitive elements, and the processes of manufacturing the displays, according to embodiments of the invention will now be described with reference to FIGS. **11-46**. FIGS. **11-24** are directed to an example electrically controlled birefringence (ECB) LCD display using amorphous silicon (a-Si). FIGS. **25-34** are directed to an example IPS LCD display using low temperature polycrystalline silicon (LTPS). FIGS. **35-43** are directed to another example IPS LCD display using LTPS. FIGS. **44-55** are directed to an example ECB LCD display using LTPS.

[0119] An example process of manufacturing an ECB LCD display according to embodiments of the invention will now be described with reference to FIGS. **11-18**. The figures show various stages of processing of two pixels, a pixel **1101** and a pixel **1102**, during the manufacture of the ECB LCD display. The resulting pixels **1101** and **1102** form electrical circuits equivalent to pixels **101** and **102**, respectively, of FIG. **1**.

[0120] FIG. **11** shows the patterning of a first metal layer (M1) of pixels **1101** and **1102**. As shown in FIG. **11**, the M1 layer for pixel **1102** includes a gate **1155***a*, a portion **1113***b* of a gate line **1113**, a lower electrode **1157***b* of a storage capacitor (not shown except for lower electrode **1157***b*), and a portion **1121***b* of an xVcom **1121**. Pixel **1101** includes a gate **1105***a*, a lower electrode **1107***b* of a storage capacitor (not shown except for lower electrode **1107***b*), a portion **1113***a* of gate line **1113**, and a portion **1121***a* of xVcom **1121**. Pixel **1101** also includes a portion **1123***a* of a yVcom **1123** (shown as dotted lines), which includes an additional portion **1140**. Portion **1123***a* has a connection point **1141** and a connection point **1143**. As shown in FIG. **11**, a gate line **1113** and an xVcom **1121** run through both pixels **1101** and **1102** in an x-direction. Gate line **1113** connects to gates **1105***a* and **1155***a*, and xVcom **1121** connects lower electrode **1107***b* and **1157***b*. Portion **1123***a* of yVcom **1123** connects to xVcom **1121** in pixel **1101**.

[0121] FIG. **12** shows a subsequent patterning step in the process of manufacturing pixels **1101** and **1102**, in which island patterns of poly-Si are formed. As can be seen FIG. **12**, the island patterns for the pixels are similar, except that semiconductor portion **1201** and **1203** of pixel **1102** are slightly different that semiconductor portions **1205** and **1207** of pixel **1101**. For example, portion **1205** is slightly smaller than portion **1201**. This is due, in part, to allow xVcom **1121** to be connected in the vertical direction (y-direction) with other xVcom lines through yVcom **1123**, as is described in greater detail below.

[0122] FIG. **13** shows connections **1301** and **1302** formed in pixel **1101**. Pixel **1102** does not include such connections. The operation of connections **1301** and **1302** is described in more detail below with reference to FIG. **14**.

[0123] FIG. **14** shows patterning of a second metal layer (M2) of pixels **1101** and **1102**. As shown in FIG. **14**, the M2 layer of pixel **1102** forms a portion **1417***a* of a green color data line, Gdata **1417** (shown as a dotted line in FIG. **14**), a source **1455***b*, a drain **1455***c*, and an upper electrode **1457***a*. Similar to pixel **1102**, the M2 layer of pixel **1101** forms a portion **1415***a* of a red color data line, Rdata **1415** (shown as a dotted line in FIG. **14**), a source **1405***b*, a drain **1405***c*, and upper electrode **1407***a*. The M2 layer of pixel **1101** also forms portions **1423***a* and **1423***b* of yVcom **1123** (shown a dotted line in FIG. **14**). Upper electrode **1407***a* is smaller than upper electrode **1457***a*, which allows portion **1423***a* to be formed in the M2 layer of the pixel **1101**. Portion **1423***a* has a connection point **1441**, and portion **1423***b* has a connection point **1443**.

[0124] FIGS. **11**, **13** and **14** together illustrate that pixel **1101** includes a vertical common line (yVcom **1415**) that allows connection of xVcom **1121** with other xVcom lines in the vertical direction (y-direction). In particular, the figures show portion **1423***a* is connected to portion **1123***a* through connection **1301** at connection points **1441** and **1141**, respectively. Portion **1123***a* is connected to **1423***b* through connection **1302** at points **1143** and **1443**, respectively. Thus, the figures show a continuous portion of yVcom **1123** is formed in pixel **1101** by the connection of multiple structures of the pixel. As shown FIG. **11**, yVcom portion **1123***a* is connected to xVcom portion **1121***a*. Consequently, the structure of pixel **1101** shown in the figures allows connection in the vertical direction of multiple xVcom lines.

[0125] FIG. **15** shows planarization (PLN) contact layers **1501** and **1503** of pixels **1101** and **1102**, respectively. FIG. **16** shows reflector (REF) layers **1601** and **1603** of pixels **1101** and **1102**, respectively. FIG. **17** shows passivation (PASS) contacts **1701** and **1703** of pixels **1101** and **1102**, respectively. FIG. **18** shows semi-transparent conductive material, such as IPO, layers that form pixel electrodes **1801** and **1803** of pixels **1101** and **1102**, respectively.

[0126] FIG. **19** shows a plan view of completed pixels **1101** and **1102**. FIGS. **20**A-B illustrate side views of completed pixel **1101** take along the paths shown in the top views shown in the figures. FIGS. **20**C-D illustrate side views of pixels **1102** and **1101** along the lines shown in FIG. **19**.

[0127] FIG. **20**A shows a side view of pixel **1101**. The portion of the M1 layer shown in FIG. **20**A includes gate line portion **1113***b*, gate **1155***a*, lower electrode **1157***b*, and xVcom portion **1121***b*. The poly-Si layer shown in FIG. **20**A includes poly-Si **1205** and poly-Si **1201**. The M2 layer shown in FIG. **20**A includes source **1455***b*, drain **1465***c*, and upper electrode **1457***a*. FIG. **20**A also shows planarization layer **1503**, reflector layer **1603**, passivation contact **1703**, and transparent conductor layer **1103**.

[0128] FIG. **20**B shows another side view of pixel **1101**. For the sake of clarity, the planarization contact, reflector, passivation contact, and transparent conductor layers are not shown in the figure. The M1 layer shown in FIG. **20**B includes gate line portion **1113***a*, gate **1105***a*, lower electrode **1107***b*, and xVcom portion **1121***a*. FIG. **20**B also shows an adjacent pixel **2001**, which has the same structure as pixel **1101**. The poly-Si layer shown in FIG. **20**B includes poly-Si portion **1211** and poly-Si portion **1207**. The M2 layer shown in FIG. **20**B includes source **1405***b*, drain **1405***c*, and upper electrode **1407***a*.

[0129] FIG. **20**C shows a side view of pixel **1102** along the line shown in FIG. **19**. The M1 layer shown in FIG. **20**C includes gate line portion **1113***b*, gate **1155***a*, and xVcom portion **1121***b*. FIG. **20**C also shows a gate insulator **2003**